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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/675,549 | 09/30/2003 | Jong-Hoon Oh | 2003P52595US | 6527 |

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| EXAMINER | |
|---|---|
| NGUYEN, VAN THU T | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2824 | |

DATE MAILED: 04/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

SDM

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/675,549 | OH, JONG-HOON | |
| | Examiner | Art Unit | |
| | VanThu Nguyen | 2824 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

1. Claims 1-40 are pending.

### *Claim Rejections - 35 USC § 112*

2. Claim 18 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Specification does not disclose a line propagating DQS signal separated from a line propagating the WAIT signal.

### *Claim Rejections - 35 USC § 103*

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. **Claims 1-2, 5-9, 11-21** are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (PGPub. 2004/0022095) in view of Nystuen et al. (referring here as Nystuen, U.S. Patent No. 6,603,706).

**Regarding claim 1**, Lee discloses, in FIGS. 1-3, a method of operating a double data rate memory device, comprising:

providing lines (lines for transmitting strobe signals SDtM 166 for data read and SDfM 168 for data written, see FIG. 1) in a system bus of the memory device to transmit a WAIT_DQS signal (strobe signal SDtM 166 and its' delayed strobe signal SDfM 168,

see FIG. 2), the WAIT_DQS signal comprising functionality of (i) a WAIT signal indicating when valid data is present on a data bus in Read cycle and when a memory is ready to accept data in Write cycle, and (ii) a data strobe (DQS) signal serving as a timing signal for valid data (see FIG. 2); and

propagating the WAIT_DQS signal in a line in a system bus of the memory device, wherein the bi-directional line is coupled to the memory (120, see FIG. 1) and a system controller (140, see FIG. 1).

However, Lee does not disclose that lines for transmitting strobe signals SDtM 166 and SDfM 168 being combined into one bi-directional line.

Nystuen discloses, in FIG. 1, a strobe signal DQS is transmitted via a bi-directional bus (see column 3, lines 8-9).

Since Lee and Nystuen are both from the same field of endeavor, the purpose disclosed by Nystuen would have been recognized in the pertinent art of Lee.

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to use a bi-directional bus disclosed in Nystuen for transmitting strobe signals SDtM and SDfM in Lee for the purpose of reducing number of pins in a memory.

**Regarding claim 2**, Lee discloses the memory comprises at least one component memory (memory 120 itself) configured to initiate the WAIT_DQS signal (via driver DRV6, see FIG. 3) and respond to the received WAIT_DQS signal (via buffer BUF3, see FIG. 3).

**Regarding claims 5 and 11**, Lee discloses, in FIG. 3, the strobe signal SDfM is driven via driver DRV6 by memory 120; and strobe signal SDtM is driven via driver DRV3 by system controller.

**Regarding claims 6-9, and 12-14**, see Nystuen, FIG. 1-2, portion with Timing With Additional Delay on DQ and DQS, or Lee, FIG. 2 with inherent latency features.

**Regarding claims 15-17, 19-21**, they are rejected under same rationale because they recite similar subject matters as in claims 1-2, 5-8, 11-14 except in apparatus format.

**Regarding claim 18**, Lee discloses SDtM/SDfM signal having both properties of WAIT and DQS signals.

5. **Claims 3 and 22** are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee in view of Nystuen further in view Kuge (U.S. Patent No. 6,466,496).

Lee and Nystuen discloses, as applied in prior rejection of claim 1 all claimed subject matters, except further limitations as set forth in claim 3.

**Regarding claim 3**, Kuge discloses, in FIG. 19, a memory processing system comprising memory components (900A-900C); a system controller (902); and a pull-up resistor R1 which couples data transmission lines with power line Vtt, which is called wired logic-OR connection (see Specification of the present invention, paragraph [0032] for illustration of wire logic-OR connection)

Since Lee, Nystuen and Kuge are all from the same field of endeavor, the purpose disclosed by Kuge would have been recognized in the pertinent art of Lee and Nystuen.

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to add a pull-up resistor to the memory device disclosed in Lee/ Nystuen because it is one of the Stub Series Terminated Transceiver Logic technique (SSTL2) which is widely used in DDR-DRAMs (see column 1, lines 12-25).

**Regarding claim 22**, it is rejected under same rationale because they recite similar subject matters as in claim 3 except in apparatus format.

6. **Claims 4, 10, 23-40** are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee in view of Nystuen further in view Jakobs (PGPub. 2004/0047227).

Lee and Nystuen discloses, as applied in prior rejection of claim 1 all claimed subject matters, except further limitations as set forth in claim 4.

**Regarding claims 4 and 10**, Jakobs discloses, in FIGS. 1-2, a memory device operating in a variable CAS latency mode for both read and write operations.

Since Lee, Nystuen and Jakobs are all from the same field of endeavor, the purpose disclosed by Jakobs would have been recognized in the pertinent art of Lee and Nystuen.

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to assign the memory device with various latency for the purpose of increasing flexibility in read/write time in order to improve system performance overall. It is noted that fixed latency mode can also be applied, which depends on users.

**Regarding claims 23-40**, they are rejected under same rationale because they recite similar subject matters as in claims 1-14 except in apparatus format.

***Conclusion***

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to VanThu Nguyen whose telephone number is (571) 272-1881. The examiner can normally be reached on Monday-Friday, 8:00am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

April 25, 2005

VanThu Nguyen
Primary Examiner
Art Unit 2824